silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology; [and]

a repeating series of gate oxides, sources and drains for at least one field effect transistor formed in each of said plurality of die, said series of gate oxides, sources and drains being formed in said semiconductor substrate; and

a repeating series of gate electrodes for at least one field effect transistor formed on each of said plurality of die, said series of gate electrodes being formed on said semiconductor substrate from said layer of polycrystalline silicon.

C4

14. (Twice Amended)A thin film transistor comprising:

a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass, said semiconductor substrate having hydrogen ions implanted therein by plasma source ion implantation, wherein said semiconductor substrate is free of metal contaminants;

a layer of polycrystalline silicon formed on at least a portion of semiconductor substrate, said layer of polycrystalline silicon having a smooth morphology;

a layer of a insulating material formed on at least a portion of said layer of polycrystalline silicon;

a gate oxide, a source region and a drain region formed in said layer of polycrystalline silicon; and

a gate electrode formed on said layer of insulating material.

C3 (Twice Amended)

Remarks

Drawings:

The drawings have been objected to under 37 CFR 1.83 (a) as not showing every feature of the invention specified in the claims. Specifically, the Examiner states the source, drain, and gate all formed in the semiconductor substrate must be shown. In

addition, the semiconductor substrate, layer of silicon dioxide on the semiconductor substrate, and the layer of polycrystalline silicon on the silicon dioxide layer with the source, drain, and gate formed on the semiconductor substrate must be shown. The semiconductor substrate 12, 52, layer 14 of silicon dioxide 16, and layer 18 of polycrystalline silicon 20 are shown in the figures. The claims have been amended to recite that the source, drain, and gate oxide are formed in the semiconductor substrate. Therefore, the drawings are in compliance with 37 CFR 1.83 (a) as they show the source 56, drain 58, and gate oxide 54 in the semiconductor substrate 52. No new drawings or proposed drawing corrections are necessary as every feature of the invention specified in the claims is shown. No new matter is added as page 10, lines 25-26 provide basis.

Specification:

The specification has been objected to for failing to provide proper antecedent basis for the claimed subject matter under 37 CFR 1.75 (d) (1). Specifically, the Examiner states that the specification does not provide proper antecedent basis for a source, drain, and gate formed in the semiconductor substrate. The claims have been amended to recite that the source, drain, and gate oxide are formed in the semiconductor substrate. Antecedent basis is provided on page 10, lines 25-26. Also, the specification has been amended at page 11, line 27 to teach that a gate oxide is formed in the semiconductor substrate. Therefore, the specification is now in compliance with 37 CFR 1.75(d)(1).

The Specification has been objected to for not complying with 35 USC § 112, first paragraph. The Examiner states that the specification has not been written so as to enable a person of ordinary skill in the art to form a source and drain in a substrate where the substrate comprises silicon dioxide, quartz, or glass. The Examiner further states that the specification also has not been written so as to enable a person of ordinary skill in the art to form a layer of polycrystalline silicon on silicon dioxide by thermal oxidation.

Applicant has provided sufficient written description to enable a person of ordinary skill in the art to form a source and a drain in a substrate where the substrate comprises silicon dioxide, quartz, or glass at page 11, lines 23-25, wherein the specification teaches that the source and drain are formed by any conventional conductive doping technique currently used in the art and provides as an example as self aligned technique. This explanation is sufficient to comply with the 35 USC §112, first paragraph. The test for enablement is whether one skilled in the art could make and use the claimed invention from the disclosures in the application coupled with the knowledge available in the art. A patent application need not teach, and preferably omits, what is well known in the art. *Spectra-Physics, Inc. v. Coherent, Inc.* 3 USPQ2d 1737 (Fed. Cir. 1987).

The specification has also been written to enable a person of ordinary skill in the art to form layer of polycrystalline silicon on silicon dioxide by thermal oxidation. At page 8, lines 9-12, page 9, lines 20-21, page 13 lines 17-19, and page 14, lines 13-14, the specification teaches that the deposition method used is any manner currently used in the art. This explanation is sufficient to comply with the 35 USC §112, first paragraph. The Examiner has provided no reasoning or analysis to carry his burden of establishing a reasonable basis to question the enablement provided in the specification. The Examiner cited to passages in the specification which clearly enable those skilled in the art to practice the invention as claimed. The Examiner has provided no evidence supporting his assertions.

The Examiner states that the disclosure is objected to for informalities because page 13, line 2 should refer to figure 5 instead of figure 3. Page 13, line 2 has been amended to refer to figure 5 instead of figure 3.

Rejections under §112

Claim 10 has been rejected under 35 USC § 112, first paragraph as containing subject matter which was not enabled. Claim 10 has been amended to recite a source, a

drain and a gate oxide are formed in said semiconductor substrate to form a field effect transistor and a gate electrode is formed on said semiconductor substrate. The gate oxide 54 and gate electrode 70 are clearly shown in Figs. 2, 2A, 2B, and 2C. The formation of the gate oxide and gate electrode are described in specification at page 11, lines 9-18. Thus, claim 10, as amended is in compliance with 35 USC § 112, first paragraph.

Claims 11 and 12 have been rejected under 35 USC § 112, first paragraph. Claims 11 and 12 have been amended to recite a source, a drain and a gate oxide formed in said semiconductor substrate to form a field effect transistor and a gate electrode formed on said semiconductor substrate. As stated above, the gate oxide 54 and gate electrode 70 are clearly shown in Figs. 2, 2A, 2B, and 2C. The formation of the gate oxide and gate electrode are described in specification at page 11, lines 9-18. Thus, claims 11 and 12, as amended are in compliance with 35 USC § 112, first paragraph.

Claim 10 has been rejected under 35 USC § 112, second paragraph, as being indefinite. Specifically, the Examiner states that it is unclear whether the layer of polycrystalline silicon recited is the same layer as the gate. Claim 10 has been amended to recite that a gate electrode is formed on the semiconductor substrate from the layer of polycrystalline silicon. Basis for this amendment is provided in the specification at page 10, lines 26-27.

The Examiner further states that it is unclear whether the claimed silicon dioxide layer is the gate oxide layer 54 of figure 2 of the substrate. Therefore, no gate oxide "layer" is claimed. The gate oxide is formed in the semiconductor substrate, as recited by claim 10. Thus claim 10, as amended is in compliance with 35 USC § 112, second paragraph.

Rejections under §103

Claim 9 rejection over "Applicant's admitted prior art"

The Examiner has rejected claim 9 under 35 USC § 103(a) as being unpatentable over "Applicants admitted prior art." The Examiner is asserting that it would have been

obvious to use PSII to implant hydrogen ions in a layer of silicon dioxide on a semiconductor substrate, the motivation being to provide a layer with increased surface hardness and improved optical properties as well as avoiding metal impurities. Applicant submits that no *prima facie* case of obviousness has been established.

Applicant discusses some current technology in the Background section of the application at page 1, line 12 – page 2, line 21, which the Examiner refers to as "Applicant's admitted prior art." There is a key dispute between the Examiner and applicant over what has been "admitted" to be in the prior art. Applicant admits that Kaufman ion sources were used to implant hydrogen ions into silicon dioxide films. Applicant also admits that PSII exists as a technique used to dope various materials such as tools, aluminum cans, and artificial joints. Also, applicant does not admit that the prior art of record used PSII as a technique in fabricating semiconductor devices such as FETs and memories.

The Examiner asserts that the motivation or suggestion to combine the "admitted prior art" is to provide a layer with increased surface hardness and improved optical properties. Providing a layer with increased surface hardness and improved optical properties cannot be proper motivation or suggestion to combine the "admitted prior art" because the claimed invention does not require these properties. Rather, claim 9 recites a semiconductor with a layer of polycrystalline silicon having a smooth morphology. There is no motivation to improve surface hardness and no motivation to improve optical properties because these are not properties that are needed by the semiconductor device as claimed.

In addition, the Kaufman method is used dope a silicon dioxide film with hydrogen ions to provide a smoother and thinner polycrystalline silicon film. PSII is used to implant ions into a material to improve their wear, friction, and corrosion properties. Thus, the reasons for using the methods are very different. In fact, they teach away from one another. PSII is used to improve the friction property of a material, while the Kaufman ion source is used to provide a smoother film. A smooth surface has less

friction than a rough surface, therefore, one would not think to use PSII to provide a smooth surface for a material because PSII is known to improve the friction property of a material. There is no indication that the PSII would be expected by one skilled in the art to provide a successful way of implanting hydrogen ions which would provide a smooth surface morphology for subsequently deposited polysilicon layer in a semiconductor device precursor.

The Examiner asserts that only routine substitution of one known equivalent technique for another is required. However, these techniques are not equivalents, but very different methods for treating materials. The Kaufman ion source uses a metal grid to bombard a silicon dioxide film with hydrogen ions. The result is a silicon dioxide film doped with hydrogen ions and metal. The Examiner admits that the "admitted prior art" does not teach the layer of silicon dioxide being free of metal contaminants. PSII implants ions from an ionized plasma around a material in an enclosed chamber. A high voltage pulse is applied to the material which drives the ions from the plasma into the surfaces of the substrate simultaneously with out manipulating the substrate. Clearly, the Kaufman method and PSII use two completely different approaches to implant ions into a target.

Applicant submits that it would not have been obvious to one of ordinary skill in the art to use PSII to implant the hydrogen ions because the prior art does not teach or suggest using the same methods to obtain the same desired result as the claimed invention. The Examiner has attempted to combine two unrelated teachings in an effort to arrive at the claimed invention. The mere fact that the references can be combined does not render the resultant combination obvious unless that prior art also suggests the desirability of the combination. In re Mills, 16 USPQ2d 1430 (Fed. Cir. 1990) and MPEP §2143.01. The desirability of the combination is not suggested in the prior art, therefore, the Examiner's proposed combination is based on prohibited hindsight.

While the present invention may take steps from individual prior art teachings, the present invention produces a different invention than that taught by the prior art.

Considering that the teachings of the prior art for PSII are not applicable to the teachings of the prior art for the Kaufman ion source, the Examiner has used prohibited hindsight in order to combine the prior art teachings in the Background section of the application. Because the prior art does not teach or suggest the invention as recited in claim 9, and the prior art does not express any desirability or motivation to combine their teachings, nor provide any expectation of success, the Examiner has failed to establish the necessary prima facie case for obviousness.

Rejection of claims 10-12 over Burns et al. in view of "Applicant's admitted prior art"

Claims 10-12 have been rejected under 35 USC §103(a) as being unpatentable over Burns et al. in view of applicant's "admitted prior art." The Examiner asserts that Burns et al. teaches a field effect transistor having a substrate with a layer of silicon dioxide over the substrate and that the layer of silicon dioxide is covered by a layer of polycrystalline silicon, pointing to page 381 and Figure 9.8 of Burns et al. The Examiner also admits that Burns et al. does not teach implanting hydrogen ions into the silicon dioxide.

Burns et al. teaches a field effect transistor with a thin oxide layer formed so that polysilicon rows can act as an effective gate over the region. The "admitted prior art" is explained above. Claim 10 recites a field effect transistor that includes "a layer of silicon dioxide having been doped with hydrogen ions deposited by a plasma source ion implantation process, wherein said layer of silicon dioxide is free of metal contamination in the layer."

As shown above, there is no motivation or suggestion in the "admitted prior art" to use PSII to implant hydrogen ions in a silicon dioxide film to permit the later deposition of a polysilicon layer with a smooth morphology. Burns et al. does not cure this deficiency. In fact Burns et al. does not even teach or suggest anything related to a smooth surface morphology with no metal contamination or the use of PSII to implant hydrogen ions. Thus, the "admitted prior art" and Burns et al. cannot properly be combined to render claims 10-12 obvious.

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Claim 14 rejection over Murata et al. in view of "Applicant's admitted prior art"

The Examiner also rejected claim 14 under 35 USC §103(a) as being unpatentable over Murata et al. (US Patent No. 5,576,229) in view of "Applicant's admitted prior art." The Examiner claims that Murata et al. and the prior art are combinable because they are from the same field of endeavor and that at the time of the invention it would have been obvious to a person ordinary skill in the art to implant hydrogen ions into the glass substrate. The Examiner asserts that the motivation for combining the references is to prepare the surface of the glass substrate for the deposition of a layer of polycrystalline silicon in order to provide for a thinner and smoother polycrystalline silicon film. The Examiner further states that it would have been obvious to a person of ordinary skill in the art to implant the hydrogen atoms by PSII. The motivation is to provide a layer with increased surface hardness and improved optical properties as well as avoiding metal impurities.

Murata teaches at figure 6E a microcrystalline silicon film 502 that includes source and drain regions 507a and 507b that are doped with impurity ions. Also shown is a channel region 507 not doped with impurity ions that is formed on a substrate 501. An insulating film 503 is formed to cover the microcrystalline silicon film 502. An interlevel insulating film 508 is formed to cover the gate electrode 504. The "admitted prior art" is explained above.

As discussed above, there is no motivation or suggestion in the "admitted prior art" to use PSII to implant hydrogen ions in a silicon dioxide film to permit the later deposition of a polysilicon layer with a smooth morphology. Murata et al. does not solve the deficiency of the "admitted prior art." In fact Murata et al. does not even teach or suggest anything related to a smooth surface morphology with no metal contamination. Thus, the "admitted prior art" and Murata et al. cannot be properly be combined to render claim 14 obvious.

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In CONCLUSION

Applicants respectfully submit that, in view of the above remarks, the application is now in condition for allowance. Early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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